Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 6 and Fig. 8.

This first sheet, which includes Fig. 5-6, replaces the original sheet including Fig. 5-6. In Figure 6, "NO" between step 62 and step 64 and "YES" between step 62 and step 70 have been switched.

This second sheet, which includes Fig. 7-8, replaces the original sheet including Fig. 7-8. In Figure 8, "NO" between step 112 and step 114 and "YES" between step 112 and step 120 have been switched.

Attachment: Replacement Sheet 2 pages

REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claim Rejections – 35 USC 102

Claims 1-22 are rejected under 35 U.S.C 102 (e) as being anticipated over Delvaux et al. (U.S. Patent No. 6,971,057), hereinafter referring to as Delvaux.

Response:

Claim 1

claim 1 recites:

> 1. An apparatus for forming a sequence of N-byte second words from bytes forming a sequence of N-byte first words, where N is any integer greater than 1, the apparatus comprising:
>
> a main memory for storing a plurality of bytes, each at a separate address,;
>
> a cache memory for storing a plurality of bytes, each at a separate address, wherein and the size of the main memory is larger than that of the cache memory; and
>
> a control circuit, coupled to the main memory and the cache memory, **for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal**, for writing bytes of each first word into either the main memory or the cache memory **according to the control signal**, for transferring bytes between the main memory and the cache memory, for reading bytes out of the cache memory or the main memory and forming each second word there from **according to the control signal** such that each second word comprises bytes of more than one of the first words.

(*Emphasis added*). Claim 1 patently defines over the prior art of record for at least the reason that the prior art of record fails to disclose the features emphasized above.

As reflected above, amended claim 1 defines an apparatus for forming a sequence of N-byte second words from bytes forming a sequence of N-byte first words. The apparatus comprising: a main memory, a cache memory, and a control circuit. The control circuit is coupled to the main memory and the cache memory for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal, for writing bytes of each first word into either the main memory or the cache memory according to the control signal, for reading bytes out of the cache memory or the main memory and forming each second word there from according to the control signal such that each second word comprises bytes of more than one of the first words.

In contrast, Delvaux discloses a method and apparatus for data interleaving/de-interleaving. The apparatus may be implemented with a controller, a first array, and a second array. The first array identifies a maximum depth value for each of a plurality of memory segments responsive to both a block data length and the desired interleaving/de-interleaving depth. The second array comprises an index associated with each of the plurality of memory segments that may be used to derive write and read addresses. The method can be described as: identifying a block data length, N, and an interleaver/de-interleaver depth, D; initializing a set of pointers associated with each of N memory segments; initializing a set of pointer maximum values responsive to the relative magnitude of N and D; identifying a memory index responsive to a base address and the set of pointer maximum values; using a memory segment identifier, a word identifier, and a byte identifier along with the memory index and the pointers to write/read the bytes of code words. (see abstract).

Tutt fails to disclose (or even to suggest) The control circuit is used for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal, for writing bytes of each first word into either the main memory or the cache memory according to the control signal, for reading bytes out of the cache memory or the main memory and forming each

second word there from according to the control signal such that each second word comprises bytes of more than one of the first words, as recited in the amended claim 1.

As such, amended claim 1, as well as claims 1-11, and 23-24 dependent therefrom, patently defines over the cited art.

Claim 12

As reflected above, amended claim 12 has limitations similar to the defining limitations of amended claim 1. Thus, independent claim 12, as well as claims 13-21, and 25-26 dependent therefrom, is patentable over the cited art.

Claim 22

Claim 22 has been canceled without prejudice.

Summary:

For at least the foregoing reasons, all pending claims are in condition for allowance. In addition, Applicant sets for the following additional comments with regard to other references cited by the Office Action.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Winston Hsu/ Date: 02.26.2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)